AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Previously Presented) A method of manufacturing a system-on-chip semiconductor device, including a CMOS logic circuit and a DRAM on the same semiconductor chip, comprising the steps of:

providing a CMOS logic circuit portion and a DRAM portion of a substrate;

forming a first transistor on said substrate at said CMOS logic circuit portion;

forming a second transistor on said substrate at said DRAM portion;

forming an interlayer film on said substrate at said CMOS logic circuit portion and on said substrate at said DRAM portion, covering said first transistor and said second transistor;

forming a groove in said interlayer film by removing a portion of said interlayer film at said DRAM portion;

forming a first polysilicon film on an upper surface of said interlayer film at said CMOS logic circuit portion and at said DRAM portion, and a second polysilicon film on an inner wall of said groove at said DRAM portion;

forming a first HSG on a surface of said first polysilicon film and a second HSG on a surface of said second polysilicon film;

removing said first HSG and said first polysilicon film from said CMOS logic portion;

forming a capacitor dielectric film on said second HSG after removing said first HSG and said first polysilicon film from said CMOS logic portion; and

forming an upper electrode on said capacitor dielectric film.

2. (Currently Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 1,

wherein said step of forming said first transistor includes a step of forming a first gate insulating layer, and

wherein said step of forming said second transistor includes a step of forming a second gate insulating layer,

wherein said first gate insulating layer is thinner ~~that~~ than said second gate insulating layer.

3. (Previously Presented) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 2,

wherein said second transistor comprises a peripheral circuit transistor and a switching transistor, and

wherein said peripheral circuit transistor and said switching transistor have similar structures.

4. (Original) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 3, wherein said step of forming an interlayer film comprises steps of:

forming a first interlayer film comprising a silicon oxide layer; and thereafter

forming a second interlayer film comprising a BPSG film.

5. (Original) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 4, further comprising steps of:

forming an opening in said first interlayer film over a diffusion region of said switching transistor; and

forming a capacitor electrode in said opening in said first interlayer film,

wherein said capacitor electrode is connected to said diffusion region of said switching transistor.

6. (Original) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 5, wherein said groove is formed in said second interlayer film, and said second polysilicon is connected to said capacitor electrode.

7. (Previously Presented) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 6, further comprising steps of:

forming a first photoresist layer on said first HSG and a second photoresist layer on said second HSG; and

removing said first photoresist layer to expose said first HSG.

8. (Cancelled)

9. (Previously Presented) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 7, wherein said capacitor dielectric film comprises a Ta_2O_5 film.

10-11. (Cancelled)

12. (Original) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 2, wherein said step of forming an interlayer film comprises a step of forming a BPSG film.

13. (Original) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 12, wherein said step of forming an interlayer film further comprises a step of forming a silicon oxide layer prior to forming said BPSG film, wherein said BPSG film is formed on said silicon oxide film.

14. (Cancelled)

15. (Original) The method of manufacturing a system-on-chip semiconductor device as claimed in claim [[14]] 1, wherein said surface area of said memory cell portion is 50 to 60% of the surface area of said DRAM portion.

16. (Currently Amended) A method of manufacturing a system-on-chip semiconductor device [[including]] that includes a CMOS logic circuit portion and a DRAM portion on ~~the~~ a ~~same~~ single semiconductor chip, said DRAM portion comprising a memory cell portion and a peripheral circuit portion, said DRAM portion comprising a cylinder type capacitor, the method comprising the steps of:

~~providing a CMOS logic circuit portion and a DRAM portion on a substrate;~~

forming a first transistor on ~~said~~ a substrate at said CMOS logic circuit portion;

forming a second transistor on said substrate at said DRAM portion;

forming an interlayer film on said substrate at said CMOS logic circuit portion and on said substrate at said DRAM portion, covering said first transistor and said second transistor;

forming a groove in said interlayer film by removing a portion of said interlayer film at said DRAM portion;

forming a polysilicon film on said interlayer film at said CMOS logic circuit portion and at said DRAM portion, and on an inner wall of said groove at said DRAM portion;

forming an HSG on a surface of said polysilicon film;

removing said HSG and said polysilicon film from an upper surface of said interlayer film from said CMOS logic portion, retaining at least a portion of said HSG in said groove and at least a portion of said polysilicon in said groove; and

forming a capacitor dielectric film on said portion of said HSG in said groove and on said exposed surface of said interlayer film, after removing said HSG and said polysilicon film.

17. (Currently Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 16,

wherein said step of forming said first transistor includes a step of forming a first gate insulating layer, [[and]]

wherein said step of forming said second transistor includes a step of forming a second gate insulating layer, and

wherein said first gate insulating layer is thinner ~~that~~ than said second gate insulating layer.

18. (Original) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 17, wherein said step of forming said first transistor further comprises steps of:

forming a first gate electrode comprising polysilicon; and

doping the polysilicon of the first gate electrode with boron,

wherein said first transistor comprises a p-channel transistor having said first gate.

19. (Original) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 17, wherein said step of forming an interlayer film comprises a step of forming a BPSG film.

20. (Currently Amended) The method of manufacturing a system on chip semiconductor device as claimed in claim 2, wherein said first transistor comprises a p-type transistor having a

gate electrode which is made of polysilicon doped with boron, and an n-type transistor having a gate electrode which is made of polysilicon doped with phosphorous.

21. (Currently Amended) The method of manufacturing a system on chip semiconductor device as claimed in claim 20, wherein said second transistor comprises a p-type transistor having a gate electrode which is made of polysilicon doped with phosphorous.

22. (Previously Presented) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 1,

wherein said step of removing said first HSG and said first polysilicon film comprises a step of exposing a part of said interlayer film; and

said step of forming said capacitor dielectric film comprises a step of forming a first capacitor dielectric film on said part of said interlayer film and a second capacitor dielectric film on said second HSG after removing said first HSG and said first polysilicon film; and

wherein said step of forming an upper electrode comprises a step of forming an upper electrode on said first capacitor dielectric film and said second capacitor dielectric film.

23. (Cancelled)

24. (New) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 1,

wherein a surface area of said memory cell portion is in a range of 10 to 25 percent of a chip surface area which is a sum of the DRAM portion and the CMOS logic portion.

25. (New) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 16,

wherein a surface area of said memory cell portion is in a range of 10 to 25 percent of a chip surface area which is a sum of the DRAM portion and the CMOS logic portion.